## REMARKS

The Examiner's Office Action mailed on December 22, 2004 has been received and its contents carefully considered.

Claims 1-20 are pending in this application. Claims 1, 8 and 15 are the independent claims.

The Applicants acknowledge with appreciation the Examiner's early indication that claims 1-7 are allowed, and that claims 11-14 and 18-20 would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

In the Action, claims 8-10 and 15-17 are rejected under 35 U.S.C. §103(a) as being obvious over Moon et al. (U.S. Patent No. 5,666,458) in view of Nakano et al. (U.S. Publ. No. 2002/0011985). The rejection is respectfully traversed.

With regard to the rejected claims, the Examiner asserts that Moon teaches an image processing apparatus (Figure 2) comprising a memory circuit (201) having a capacity of n, the memory circuit storing an input data (output from the A/D converter 200) in response to a write address (output from 204) and outputting an output data in response to a read address (output from 205); a write control circuit (204) coupled to the memory circuit and the counter, the write control circuit generating the write address in response to the sampling clock signal (from sampling frequency input), the horizontal synchronization signal and the counting signal; and a read control circuit (205) coupled to the memory circuit and the write control circuit, the read control circuit generating the read address in response to the write address, the sampling clock signal (from sampling frequency input) and a phase difference signal representing n/2 (column 3, lines 20-32).

While Moon does disclose a 1H line memory circuit (201), a write address generator (204) and a read address generator (205), the Applicants disagree with the Examiner's contention that these correspond in all respects to the elements recited in the rejected claims. With respect to the recited read control circuit, for example, the read address generator (205), shown in Figure 2 of Moon, **is not connected to** the write

address generator (205), as claims 8 and 15 require. Further, the read address generator (205) **does not receive** the write address and the sampling frequency input, as the independent claims require. Moreover, the write address generator (205) **does not receive** a phase difference signal representing n/2, as claim 8 specifically requires.

The Examiner points specifically to column 3, lines 20-32 of Moon for support. In this portion, the relevant sentence reads: "Within the 1H line memory 201 the reading of storage locations is arranged to take place with an offset from their being written, which offset averages about one-half scan line." It is respectfully submitted that this sentence fails to suggest in any way the recited phase difference signal representing n/2.

As is clear from the referenced figure and text, the read address generator (205) in Moon receives only a read clock, and no other signal. Therefore, Moon fails to teach or suggest the read control circuit of the claimed invention. Moreover, Moon discloses that "[t]he error with respect to time base is corrected by reading with the stable read clock while writing into the 1H line memory 201 in accordance with the sampling frequency input that closely tracks the jitter of the input video signal" (column 3, lines 24-31). Thus, it is understandable that the structure of the circuit in Moon would reflect a method of time base correction that is significantly different from that of the present invention.

In the Action, the Examiner acknowledges that Moon fails to explicitly teach or suggest a counter for counting a sampling clock signal. The Examiner points to Nakano as teaching a counter (104) and argues that it would have been obvious to one of ordinary skill in the art of time the present invention was made to combine the teachings of Nakano into the system of Moon in order to count the proper number of clock signals and thus to output the read and write control circuits.

The Applicants respectfully disagree. Nakano shows a horizontal counter (104) in Figure 1. The horizontal counter (104), which is part of the Nakano's synchronization signal generation circuit 401, samples the clock signal from the oscillation circuit (103) (paragraph [0063], lines 2-5). However, the purpose of the synchronization signal generation circuit 401is to generate a vertical synchronization signal and a horizontal synchronization signal based an externally-supplied vertical

synchronization signal (paragraph [0062], lines 3-8), rather than an external horizontal synchronization signal as recited in the rejected claims. Therefore, it is not understand why one of ordinary skill in the art would be motivated to combine the teachings of Nakano into the system of Moon. Even if the references were combined, as the Examiner proposes, the combination would not result in the present invention because Nakano does not overcome Moon's failure, as discussed above, to disclose the read control circuit recited in the claims.

For at least the foregoing reasons, it is respectfully submitted that claim 8, as well as dependent claims 9-14, patentably distinguish over the applied references, whether considered individually or in combination. Further, it should also be clear from the forgoing that independent claim 15, as well as dependent claims 16-20, also patentably distinguish over the applied prior art. Accordingly, withdrawal of the Examiner's rejection and allowance of all of pending claims 1-20, are respectfully requested.

Should the Examiner feel that an interview would help to expedite the prosecution of this application, the Examiner is hereby encouraged to contact the undersigned counsel to arrange for such an interview.

Respectfully submitted,

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Date

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